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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,023	07/30/2001	Paul J. Mantey	10016249-1	1038

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	2

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/918,023	MANTEY ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondenc address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 July 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: The serial numbers of the applications incorporated by reference are missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 12 recites the limitation "the first serial bus" and "the second serial bus" in lines 1 and 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Botelho('544).

6. Regarding claim 1, admitted prior art discloses a method of in-system programming of EEPROMs, the EEPROMs coupled to provide configuration code to programmable logic devices(Paragraph 11), each EEPROM being located on a particular circuit board of a plurality of circuit boards of a system and wherein not all

EEPROMs are located on the same circuit board(Figure 1), comprising: providing a plurality of board-specific serial busses(Figure 1, 111 & 126), each board-specific serial bus coupling to EEPROMs of a particular circuit board(Figure 1); erasing at least one EEPROM coupled to the particular board-specific serial bus; and writing programmable logic device configuration code through the selected board-specific serial bus to the at least one EEPROM(Paragraph 12).

The background does not disclose coupling the plurality of board-specific serial busses to a common configuration point having selection apparatus; coupling the common configuration point to configuration apparatus capable of interacting with at least one serial bus to program EEPROMs; setting the selection apparatus to select a particular board-specific serial bus of the plurality of board-specific serial busses.

However, Botelho discloses a common configuration point(Figure1, 12) coupled to a configuration apparatus(Figure 1, 14) with a selection apparatus(Figure 1, 36) interacting with at least one bus to test a unit(Figure 1, 16); setting the selection apparatus to select particular bus of a plurality of units(Column 2, Lines 23-27). Therefore, it would have been obvious to combine admitted prior art with the teachings of Bothelho because it would save manpower and time in connecting and disconnecting the configuration system(Column 1, Lines 32-35).

7. Regarding claim 2, admitted prior art discloses that the plurality of board-specific serial busses are of the JTAG type(Paragraph 11).

8. Regarding claim 3, admitted prior art discloses that the programmable logic device configuration code comprises configuration code for at least one FPGA(Paragraph 11).

9. Regarding claim 4, admitted prior art discloses the step of accessing the particular board-specific serial bus to verify compatibility of the code file with the selected circuit board(Paragraph 13).

10. Regarding claim 5, admitted prior art discloses at least one EEPROM device is collocated on the same die as at least one FPGA(Figure 1).

11. Regarding claim 6, admitted prior art discloses the step of loading at least one of the programmable logic devices with configuration code from at least one of the EEPROMs(Paragrapgh 12).

12. Regarding claim 7, admitted prior art discloses an in-system programming of EEPROMs, at least some of the EEPROMs coupled to provided code to programmable logic devices,(Paragraph 11), each EEPROM located on a particular circuit board of a plurality of circuit boards of a system and where not all EEPROMs are located on the same circuit board(Figure 1): comprising a serial bus intended for coupling to EEPROMs of a particular circuit board(Figure 1)

Admitted prior art does not disclose a common connection point apparatus for a plurality of serial busses and connecting to a configuration system; selection apparatus for selecting a particular bus of the plurality of serial busses; and coupling apparatus for coupling signals from the configuration system to the particular bus of the plurality of serial busses.

However, Botelho discloses a common configuration point(Figure 1, 12) for a plurality of serial busses coupled and connecting to a configuration system(Figure 1, 14). Botelho further discloses a selection apparatus(Figure 1, 36) for selecting a particular bus of the plurality of serial busses(Column 2, Lines 23-27). Botelho also discloses a coupling apparatus(Figure 1, 12) for coupling signals from the configuration system to the particular bus of the plurality of serial busses(Figure 1). Therefore, it would have been obvious to combine admitted prior art with the teachings of Bothelho because it would save manpower and time in connecting and disconnecting the configuration system(Column 1, Lines 32-35).

13. Regarding claim 8, admitted prior art discloses the serial busses being JTAG busses(Paragraph 11).

14. Regarding claim 9, Botelho discloses the selection apparatus that comprises a switch settable by a technician(Column 4, Lines 25-26). A technician has to initialize the tester and therefore would set the switch on the apparatus.

15. Regarding claim 10, Botelho a selection apparatus that comprises a register addressable by the configuration apparatus(Figure 1, 32).

16. Regarding claim 11, admitted prior art discloses a system comprising: a plurality of interconnected circuit boards(Figure 1, 100 and 102), at least two of the plurality of interconnected circuit boards embodying at least one FPGA(Figure 1, 104) coupled to a configuration EEPROM(Figure 1, 108) of the type capable of being programmed over a serial bus; wherein at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a first serial bus(Figure 1, 108), and at least one EEPROM of a

circuit board of the plurality of circuit boards is coupled to a second serial bus(Figure 1, 126).

The admitted prior art does not disclose a common configuration point apparatus coupled to the first serial bus and to the second serial bus, the common configuration point apparatus further comprising: selection apparatus for selecting a particular bus of the first and second serial busses; and coupling apparatus for coupling configuration signals to the particular bus of the plurality of serial busses.

However, Botelho discloses a common configuration point apparatus(Figure 1, 12) coupled to the first serial bus and to the second serial bus(Figure 1, 28 and 30), the common configuration point apparatus further comprising: selection apparatus(Figure 1, 36) for selecting a particular bus of the first and second serial busses(Column 2, Lines 23-27); and coupling apparatus for coupling configuration signals to the particular bus of the plurality of serial busses(Figure 1). Therefore, it would have been obvious to combine admitted prior art with the teachings of Bothelho because it would save manpower and time in connecting and disconnecting the configuration system(Column 1, Lines 32-35).

17. Regarding claim 12, admitted prior art discloses the first serial bus and the second serial bus are of the JTAG type(Paragraph 11).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Adams et al.(US Publication 2003/0120974) discloses a method for testing multiple devices through a common connection apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Nimesh G Patel
Examiner
Art Unit 2112

NP
NP

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100